High-Performance Top-Gated Organic Field-Effect Transistor Memory using Electrets for Monolithic Printed Flexible NAND Flash Memory

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High-performance top-gated organic field-effect transistor (OFET) memory devices using electrets and their applications to flexible printed organic NAND flash are reported. The OFETs based on an inkjet-printed p-type polymer semiconductor with efficiently chargeable dielectric poly(2-vinylnaphthalene) (PVN) and high-k blocking gate dielectric poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) shows excellent non-volatile memory characteristics. The superior memory characteristics originate mainly from reversible charge trapping and detrapping in the PVN electret layer efficiently in low-k/high-k bilayered dielectrics. A strategy is devised for the successful development of monolithically inkjet-printed flexible organic NAND flash memory through the proper selection of the polymer electrets (PVN or PS), where PVN/- and PS/P(VDF-TrFE) devices are used as non-volatile memory cells and ground- and bit-line select transistors, respectively. Electrical simulations reveal that the flexible printed organic NAND flash can be possible to program, read, and erase all memory cells in the memory array repeatedly without affecting the non-selected memory cells.

1. Introduction

Recently, electronic devices manufactured by graphic art printing methods have attracted tremendous interest due to their great potential for the creation of a new paradigm in the fabrication process of low-cost, large area, flexible electronic and optoelectronic devices, such as rollable displays, plastic or paper solar cells, printed radio frequency identification (RFID) tags for item-level tagging, and interactive sensors.[1–6] Most of these flexible electronic products manufactured by printing processes consist of some basic building blocks such as digital or analogue integrated circuits (ICs), thin-film batteries, sensors, displays, and random access memory (RAM).[7] Beyond the present low-end applications, as forecasted on many technology roadmaps, the ultimate stage of printed and flexible electronics is progressing toward more complicated and sophisticated high-end products such as microprocessors and high-capacity solid-state drives (SSD).[8] For the successful development of these applications, it is obvious that all components must meet required specifications as well as be monolithically printed through a continuous roll-to-roll process.

In addition to printed ICs which have progressed remarkably in the last decade,[9–12] electrically erasable and programmable non-volatile semiconductor memory is also necessary. It must

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be manufactured using simple printing methods, have excellent architectural compatibility with peripheral logic circuits, and show superior memory performance for fast switching speed and stable long-term information storage.[13–16] Printed and flexible memory devices (including organic) can be classified as capacitor- or transistor-types.[13,16] Compared to capacitor-type, transistor memory has advantages in that it has little performance uniformity and no cross-talk problems between adjacent memory cells, and it provides for non-destructive read-out for stable data sensing and excellent compatibility with ICs.[15–17] These features originated from an operation mechanism wherein the gate field and channel conductance are modulated by stored charges either in metal and organic nano-floating gates, ferroelectrics, or charge trap gate dielectrics in organic field-effect transistors (OFETs),[16] very similar to floating-gate transistors in conventional Si-based flash memory.

The top-gate/bottom-contact OFETs and their application to organic flash memory provides crucial advantages over other device configurations. (i) The relatively easy formation of a short-channel length of source/drain (S/D) electrodes either by conventional photolithography or direct self-aligned printing enables fast switching speed and high memory capacity per unit area.[2] (ii) The auto-encapsulation of relatively sensitive organic semiconductors by upper-layered gate electrodes and dielectric increases the stability and reliability of the devices during operation under ambient conditions. (iii) The easy observation of ambipolarity by using hydroxyl-group-free polymer dielectrics, such as poly(methyl methacrylate) (PMMA) and CYTOP.[18,19] (iv) A reduction in contact resistance for charge injection from S/D electrodes into the semiconductor due to a large contact area and a decrease in the current crowding effect,[20] which enables electret and nano-floating-gate memories to show a large memory window in a short amount of switching time. It should be noted that the capability to program and erase the organic charge trap memory is critically determined by the supplementation of mobile charge carriers (electron and hole) from a semiconductor channel.[21]

Top-gate OFET memory devices are mainly demonstrated in the form of a nano-floating gate by embedding metal nano-particles into gate dielectric layers.[22,23] In our previous report, gold NPs were embedded at the interface between a layer of polystyrene (PS) and a layer of cross-linked poly(4-vinylphenol) (cPVP), and the threshold voltage (V_{Th}) of the OFET devices was reversibly and systematically controlled from negative charge trapping in the Au NPs by the application of external gate fields.[22] However, the process for the formation of a nano-floating gate is bothersome and it is relatively difficult to control the size and distribution of the NPs so that non-uniform memory characteristics are induced.[24–26] Moreover, bi-layered low-k polymer dielectric layers provide a large power consumption due to a high operating voltage. Charge trap transistor memory using electret is considered to be a much simpler approach to realize similar NFGM operations without introducing additional NFG formation processes. The organic electret memory showed stable and reliable memory operation with a short switching time, a high on/off-current ratio, and a large memory window.[27,28] However, to the best our knowledge, a top-gated OFET memory using full-polymer electret and dielectric layers has not been demonstrated.

Here we report high-performance top-gated OFET memory using a polymer semiconductor with alkyl-substituted thienylenevinylene (TV) and dodecylthiophene (PC12TV12T) and bi-layered polymer dielectrics, i.e., poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) and electrets [poly(2-vinylnaphthalene) (PVN) and polystyrene (PS)]. The PC12TV12T OFETs with PVN/P(VDF-TrFE) showed excellent non-volatile memory characteristics: an opened memory window (MW) of more than 90 V, a high on/off-current ratio (I_{on}/I_{off}) of ~10^5, a relatively low operation voltage of less than 20 V, and a long retention time of ~10^7 s, as well as a stable writing/reading/erasing cycling endurance and multi-level (two bits per one cell) memory capability. The excellent memory properties originated from efficient and reversible charge trapping and release in the PVN electret layer. However, the memory characteristics effectively disappeared after replacing PVN with PS. The PS/P(VDF-TrFE) devices showed a small open MW under low-bias conditions and a narrow MW of ~34 V even at an applied bias of more than ±90V. In the end, a facile strategy for the successful development of monolithically printed and flexible organic NAND flash memory by proper selection of polymer electrets (PVN or PS) in TG/BC OFETs, where PVN/- and PS/P(VDF-TrFE) devices are used as eight memory cells and ground- and bit-line select transistors, respectively.

2. Results And Discussion

To realize flexible printed organic flash memory (OFM) based on TG/BC OFETs with bi-layered polymer gate dielectrics, suitable selection of the 1st and 2nd gate dielectric layer materials and those orthogonal solvents is very important. We chose PVN, and P(VDF-TrFE) for the chargeable (electret) and blocking dielectric layers, respectively. Their molecular structures are represented in **Figure 1**a. The sequential deposition of three polymer layers, i.e., conjugated polymer, electret, and blocking dielectric layers, by a solution process, is quite difficult due to dissolution and swelling of the under-lying layer. We used orthogonal solvents, 2-butanone (a good solvent for both PS and PVN, but a bad solvent for an under-laid semiconductor) and acetonitrile (good solvent for P(VDF-TrFE), but a bad solvent for both PS and PVN). Triple polymer layers were successfully deposited with no intermixing (see clear step thickness profile in Figure 4a,b). P(VDF-TrFE) was used as a blocking dielectric here for low-voltage operation due to its high dielectric constant (k) (ε_r = ~10.5).[29] PVN and PS were used as a charge trap layer since those polymers showed excellent electret capability.[28] However, PVN showed better charge transfer and trapping properties than PS, presumably due to having a smaller energy gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) that is induced by its relatively extended π-conjugation compared with that of PS, and/or by the high localized deep trap density in PVN.[30]

A low-k/high-k bi-layered dielectric system enables the inducement of an efficient charge transfer from semiconductor to electret, since the applied electric field is relatively stronger in the

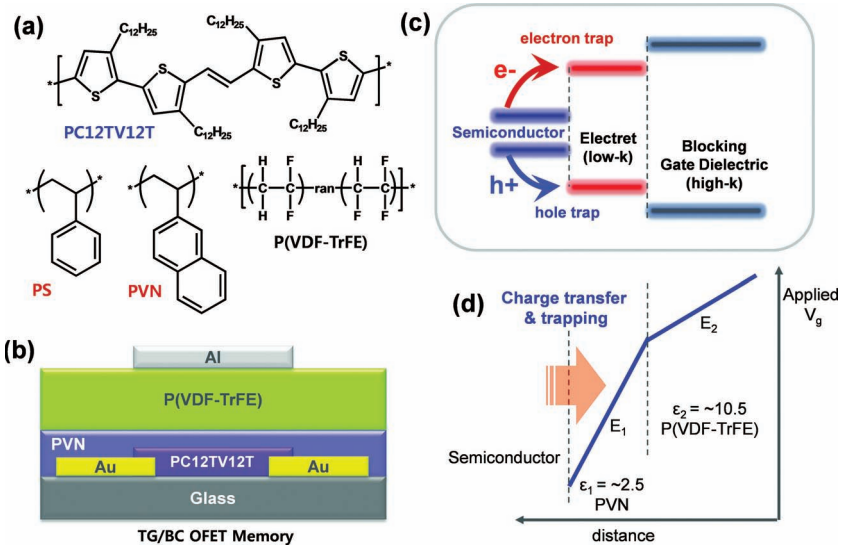

Figure 1. a) Molecular structures of the PC12TV12T, PS, PVN, and P(VDF-TrFE). b) TG/BC OFET-based memory structure. c) Schematic illustrations for charge transfer and trapping mechanisms and d) loaded electric field strength in each of the dielectric layers in top-gated OFET memory using electret.

low-k layer than in the high-k layer.[22,31] As shown in Figure 1d, the applied electric field in the first gate dielectric (electret) layer can be estimated from the following Equation (1).[32]

$$E_1 = \frac{V_g}{d_1 + d_2\left(\frac{\varepsilon_1}{\varepsilon_2}\right)} + \frac{Q}{\varepsilon_1 + \varepsilon_2\left(\frac{d_1}{d_2}\right)} \quad (1)$$

Where Q is the (negative) stored charge in the electret, ε_i are the dielectric constants and d_i the thicknesses of the two dielectric layers. At the initial stage of memory operation ($Q = 0$) during application of $V_g = 70$ V, the applied gate fields in PVN (E_1) is estimated to be about 4.6 MV/cm, which is much higher than E_2 in P(VDF-TrFE) layer of ~1.1 MV/cm. This high electric field at the interface between semiconductor and PVN enable to efficient injection of a negative charge carrier from the semiconductor and trapping in electret.

As an active layer of the OFET memory, a recently published p-type conjugated polymer containing alkyl-substituted thienylenevinylene (TV) and dodecylthiophene (PC12TV12T, the chemical structure of which is shown in Figure 1a) was used.[33] Spin-coated PC12TV12T OFETs typically exhibit a high hole mobility of up to ~1.0 cm^2/Vs.[33] As can be seen in **Figure 2**, the PC12TV12T film showed more ordered crystalline features by increasing thermal annealing temperature from pristine sample to 200 °C annealed. The charge carrier mobility of the PC12TV12T OFET [with typical poly(methyl methacrylate) dielectric] is progressively increased from 0.15, 0.28, 0.34, to 0.51 cm^2/Vs by increasing the annealing temperature from pristine, 110 °C, 150 °C, and 200 °C, respectively. These device properties are consistent with previous our report on PC12TV12T OFETs.[33] Although the morphological changes by thermal annealing of the semiconductor active layer increased the charge carrier mobilities, no significant changes in charge trapping transistor memory characteristics were observed, such as bias hysteresis (memory windows). Moreover, all fabricated memory devices with different electret layers [PS or PVN] and P(VDF-TrFE) dielectric had the same thermal annealing history near 80 °C, thus it reveals that there is no remarkable change of the memory performance on morphology of the active polymer semiconductor layer.

In the present study, all PC12TV12T active layers were patterned by inkjet-printing to produce transistor and memory

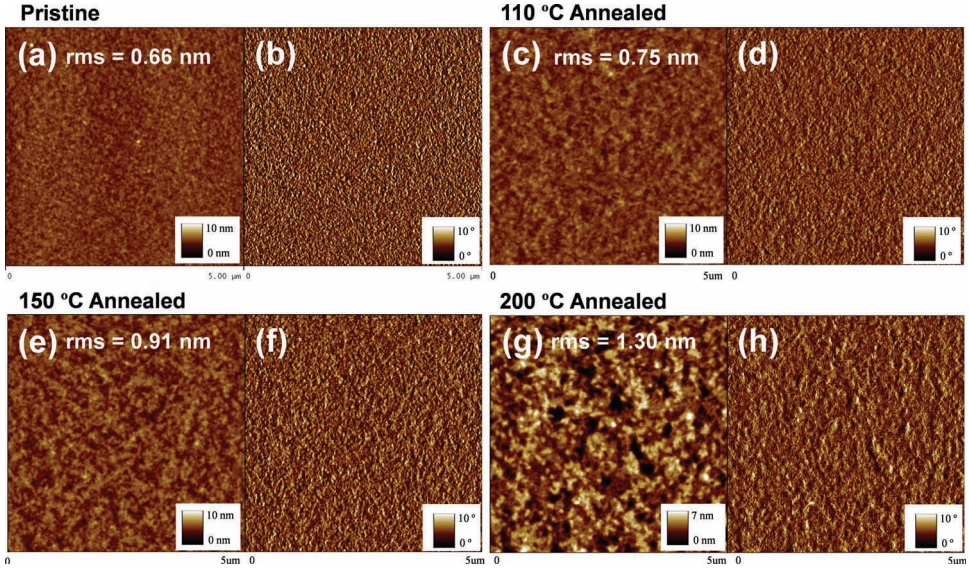

Figure 2. Atomic force microscopy (AFM) images of the PC12TV12T semiconductor layer in a,c,e,g) height and b,d,f,h) phase mode. a,b) Pristine film and after thermal annealing c,d) at 110 °C, e,f) at 150 °C, and g,h) at 200 °C for 30 min.

Table 1. Fundamental parameters of the PC12TV12T OFETs using various gate dielectric layers. Channel width/length = 1.0 mm/20 μm.

Parameters	P(VDF-TrFE)	PS/P(VDF-TrFE)	PVN/P(VDF-TrFE)
Dielectric constant	10.5	2.45/10.5	2.65/10.5
Thickness [nm]	~420	~65/~350	~70/~350
Capacitance [nF/cm^2]	~21.5	~14.9	~15.8
Linear Mobility [cm^2/Vs] (at V_d = -10 V)	~0.20	~0.11	~0.061
I_{on}/I_{off}	~10^8	~10^8	~10^7
$V_{Th,i}$ [V]	~12.4	~–11.8	~–5.4
ΔV_{Th} [V] (scanned V_g)	Negligible	~5 (±30V)	~11 (±30 V)
		~5 (±50V)	~37 (±50 V)
		~10 (±70V)	~61 (±70 V)
		~34 (±90V)	~92 (±90 V)

arrays and to minimize the off-current of the OFET. As summarized in **Table 1**, the inkjet-printed PC12TV12T OFETs with P(VDF-TrFE) and PS/P(VDF-TrFE) showed reasonably high hole mobilities of about 0.1–0.2 cm^2/Vs (obtained at the linear region at V_d = –10 V), while PVN/P(VDF-TrFE) OFET devices showed a lower hole mobility of ~0.06 cm^2/Vs due to easy charge trapping in the PVN electret layer. All devices showed high I_{on}/I_{off} ratio of $10^{7\text{-}8}$ due to an effectively patterned active area by inkjet-printing. The initial threshold voltages ($V_{Th,i}$) of P(VDF-TrFE), PS/P(VDF-TrFE), and PVN/P(VDF-TrFE) devices were about 12.4, –11.8, and –5.4 V, respectively. It was noted that the positively shifted $V_{Th,i}$ of the P(VDF-TrFE) device was attributed to charge accumulation in the active channel by –C–F dipoles near the semiconductor and dielectric interface, which is very similar behaviour to a fluorinated self-assembled monolayer in bottom-gate OFETs.[34,35]

P(VDF-TrFE) copolymer is a commonly used ferroelectric material, but our OFETs with a P(VDF-TrFE) single layer showed no significant ferroelectric memory characteristics (see negligible bias hysteresis in Figure 5a). This was attributed to the formation of a non-polar α-phase film after spin casting and low-temperature thermal annealing (~80 °C), which was far below typical thermal annealing temperature for the formation of the ferroelectric β-phase of P(VDF-TrFE) near 135 °C.[36] It should be noted here that the P(VDF-TrFE) film in this study was processed at low-temperature on purpose in order to only verify the charge trap (electret) memory characteristics without misapplication to ferroelectric memory properties. The atomic force microscopy (AFM) images in **Figure 3**a,b also confirmed no significant crystalline morphology of the as-cast low-temperature annealed P(VDF-TrFE), while the thermal annealed film at above the transition temperature clearly exhibited a needle-like crystalline surface morphology (see our previous report).[29] Moreover, Top surface morphology of the various polymer dielectrics, such as PS, PVN, P(VDF-TrFE), PS/P(VDF-TrFE), and PVN/P(VDF-TrFE), were studied by AFM measurement. As shown in Figure 3, both PS and PVN single layers showed very smooth film topology, whose root mean square (rms) roughness were only 0.26 and 0.36 nm for PVN and PS films, respectively. There are also no crystalline features both on PS and PVN. PS/P(VDF-TrFE) and PVN/P(VDF-TrFE) bi-layered films also observed no distinctive differences from P(VDF-TrFE) single layer morphology. It is attributed that P(VDF-TrFE) film does not changed by and affected to under-laid PS or PVN film morphology, since acetonitrile used solvent for dissolving P(VDF-TrFE) does not completely dissolve (orthogonal solvent) under-laid PS and PVN films (see **Figure 4**a,b). As shown in Figure 4d, all capacitance-voltage characteristics of the P(VDF-TrFE) single layer, PS/P(VDF-TrFE) and PVN/P(VDF-TrFE) bi-layer films also showed little hysteresis loop between forward and reverse voltage scans. Therefore, the P(VDF-TrFE) layer was only considered as playing the above-mentioned roles as high-k charge blocking layer to decrease operating voltage and

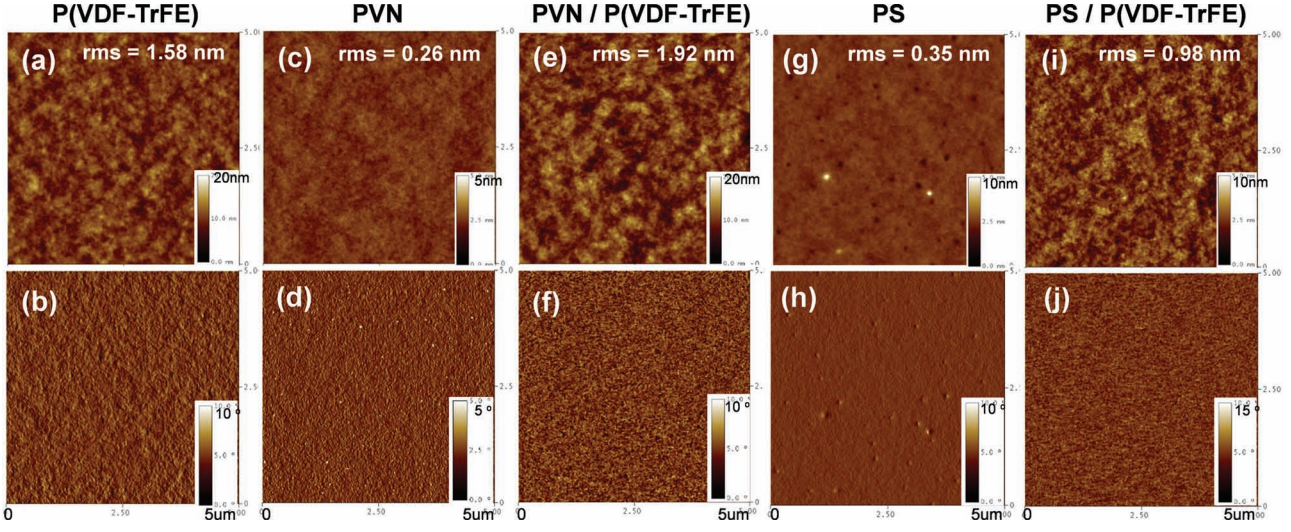

Figure 3. Atomic force microscopy (AFM) images of the spin-coated various dielectric layers in a,c,e,g,i) height and b,d,f,h,j) phase mode. a,b) P(VDF-TrFE), c,d) PVN, e,f) PVN/P(VDF-TrFE) bilayer, g,h) PS, and i,j) PS/P(VDF-TrFE) bilayer.

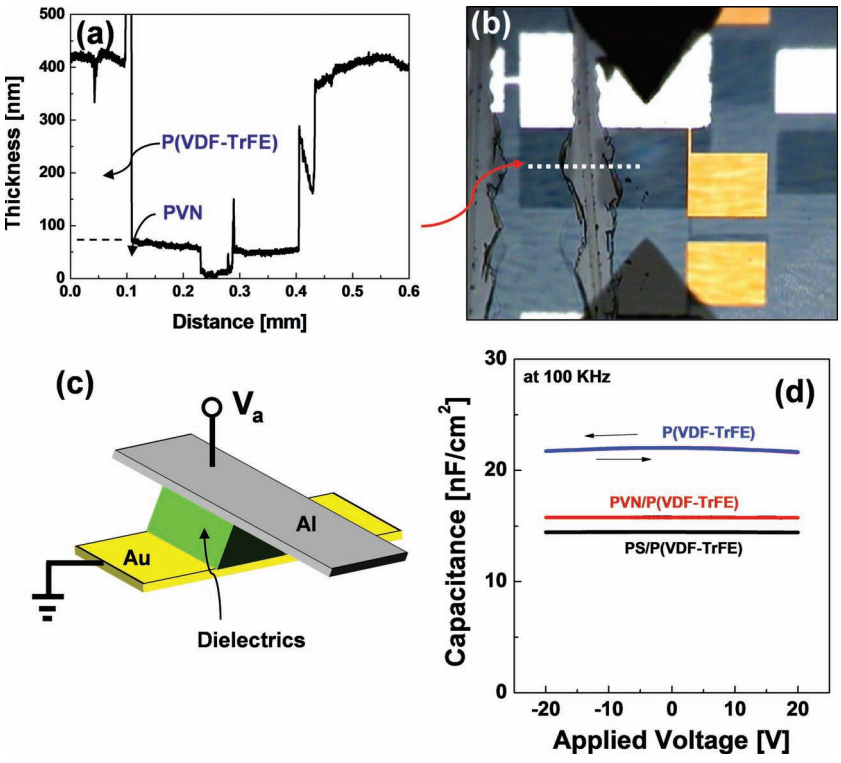

Figure 4. a) Thickness profile of the bi-layered PVN/P(VDF-TrFE) dielectrics through the dotted line in b) CCD camera image of scratched bi-layer dielectric layers. c) Device configuration for the gate dielectric capacitance vs applied voltage (CV) measurement and d) corresponding CV characteristics of the various gate dielectrics, P(VDF-TrFE), PS/P(VDF-TrFE), and PVN/P(VDF-TrFE), measured at 100 KHz.

to induce efficient charge transfer and trapping in the electret without any ferroelectric memory behaviour.

Charge trap memory characteristics were observed after insertion of PS or PVN between the PC12TV12T and the P(VDF-TrFE) layers. As **Figure 5**b,c shows, the PVN/P(VDF-TrFE) device exhibited very large MWs of more than 90 V during forward and reverse gate voltage (V_g) sweeps of ±90 V. Moreover, this device exhibited a relatively broad MW below V_g = ±30 V, and the amount of opened MW was gradually increased proportionally to the applied V_g. Even though the PS/P(VDF-TrFE) device also showed some memory characteristics, these only occurred at a V_g of greater than ±50 V and had a narrow MW of ~34 V even at V_g = ±90 V. These distinctive memory characteristics between the PS/P(VDF-TrFE) and PVN/P(VDF-TrFE) devices were attributed to a different alignment of the energy levels for the charge transfer from the semiconductor to the electret. PVN has a more extended π-conjugation length thus smaller HOMO and LUMO gaps than PS. As shown in Figure 5d–f, therefore, it was believed that the lower injection barrier for efficient charge transfer and trapping in PVN/P(VDF-TrFE) devices induced larger MWs even at lower applied

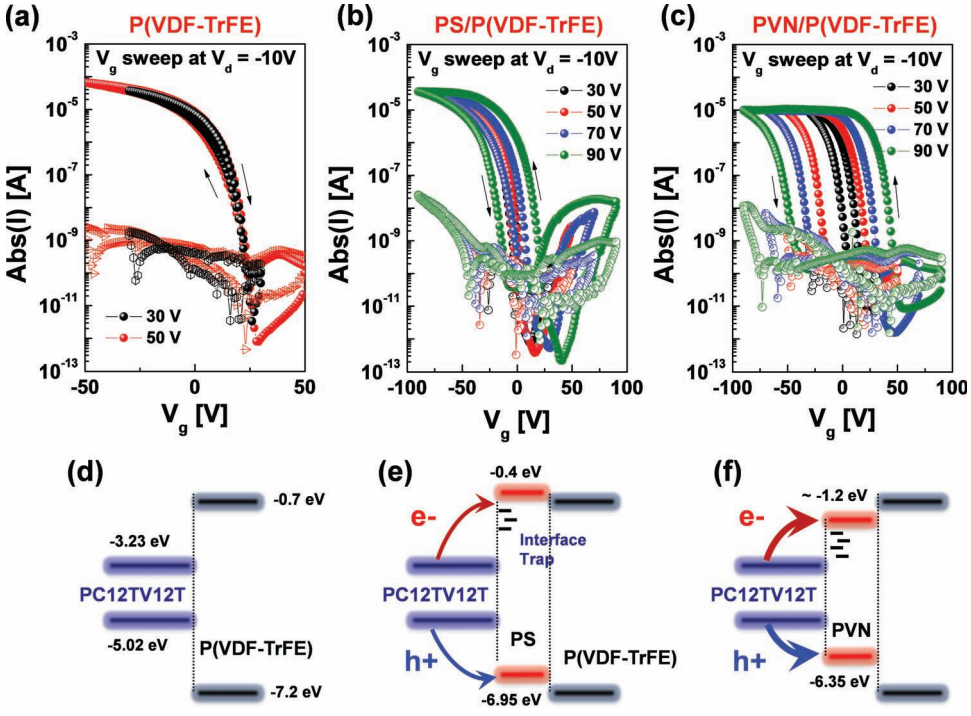

Figure 5. Transfer characteristics of the OFETs with a) P(VDF-TrFE), b) PS/P(VDF-TrFE), and c) PVN/P(VDF-TrFE) dielectrics. Schematic diagram for different modes of charge transfer and storage in each gate electret layer: d) P(VDF-TrFE), e) PS/P(VDF-TrFE), and f) PVN/P(VDF-TrFE) dielectrics [the indicated HOMO and LUMO levels are estimated from literature survey.[33,44–46]]

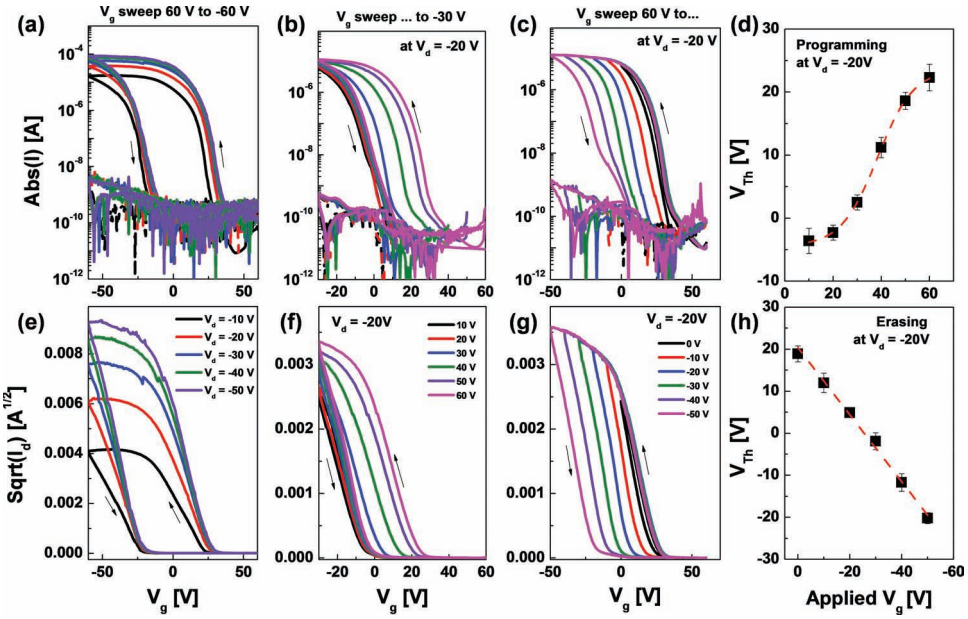

Figure 6. Memory characteristics of the PVN/P(VDF-TrFE) OFET devices. a,e) MWs opened at different V_d from –10 V to –50 V. V_g was swept back and forth from 60 V to –60 V. Controllable shifts of transfer curves b,f) during programming (V_g was swept from different voltages to –30 V) and c,g) erasing (V_g was swept from 60 V to different voltages) processes. d,h) The threshold voltage (V_{Th}) shift characteristics by application of programming and erasing gate bias (V_g), respectively.

bias than that of the PS/P(VDF-TrFE) devices.[30] In addition, it should be also noted that different amount of interface trap density between PC12TV12T semiconductor and various gate dielectrics including PS, PVN, and P(VDF-TrFE) cannot still be excluded from charging capability of the electret materials so that observed memory characteristics.

The charge memory characteristics of the PVN/P(VDF-TrFE) OFET device were verified depending on application of the source-drain (V_d) and source-gate (V_g) voltages. As shown in **Figure 6**, the onset voltage (V_{on}), threshold voltage (V_{Th}), and their amount of MWs were only changed by V_g, and obviously not by significant changes in V_d (Figure 6a,e). The high V_d only increased the drain current (I_d) and affected the I_{on}/I_{off}, where the I_{on}/I_{off} was gradually increased from ~10^5 (at V_d = –10 V) to ~10^6 (at V_d = –50 V). In Figure 6b,f, a forward positive bias was changed from V_g = 10 V to 60 V at V_d = –20 V while the reverse bias was fixed at V_g = –30 V during the programming process. The transfer curves during forward V_g scans were progressively shifted in the positive direction, where the initial V_{Th} of ~–4 V was remarkably changed to ~22 V when the programming voltage was increased from 10 V to 60 V, respectively. The erasing voltage characteristics also were similar to the programming process. A starting forward bias was fixed at V_g = 60 V and the reverse bias was increased from 0 V to –50 V at V_d = –20 V. As shown in Figure 6c,g, the V_{Th} of the transfer curves during a reverse V_g scan were proportionally shifted from ~19 V (at V_g = 0 V) to ~–22 V (at V_g = –50 V). The V_{Th} of the OFETs using PVN/P(VDF-TrFE) bi-layered dielectrics enabled systematic control by application of external gate bias. In addition to the non-volatile memory applications, OFETs with systematically controllable V_{Th} can also be used in unipolar or complementary-like electronic circuitry and in various sensors.[37,38]

The operation mechanism of charge trap OFET memory is understood as shown in **Figure 7**. First, stable and reversible bias hysteresis loops were obtained from sequential V_g scans from 50 V to –50 V and *vice versa* (see Figure 7a,b). The I_{on}/I_{off} and MW were about 10^5 and 37 V, respectively, and their hysteresis loops were very stable even after more than 100 sequential V_g scans. The reversible counter-clockwise hysteresis loops revealed the following: (i) memory behaviour originated from charge trapping in the PVN electret layer,[22] rather than from either the alignment of permanent dipoles in the P(VDF-TrFE) layer or from any structural deformation of semiconductor or gate dielectrics;[39] (ii) charge trapping and detrapping processes occurred within a fast scan time, possibly providing a high switching speed; and, (iii) positive V_{Th} and V_{on} at the initial stage of V_g > 0 V indicated that the bias hysteresis resulted from a negative charge (electron) trapping in the electret, thus the trapped electrons modulated the gate field and mobile holes accumulated at the interface of PC12TV12T and PVN layers.[27]

Schematic illustrations of the charge trapping and detrapping processes in each bias condition indicated in Figure 7b for the PVN/P(VDF-TrFE) OFET memory device are shown in Figure 7c. During the programming process, as shown in step-1 of Figure 7c, negative charge carriers (electron) were transferred from the semiconductor to the electret layer by application of positive high V_g > 0 V. The injected electrons to the electret were trapped in a very fast time scale of ~10^{-12} s. [40] The stored negative charges modulated the gate field and accumulated positive charge carriers (holes) in the interface between

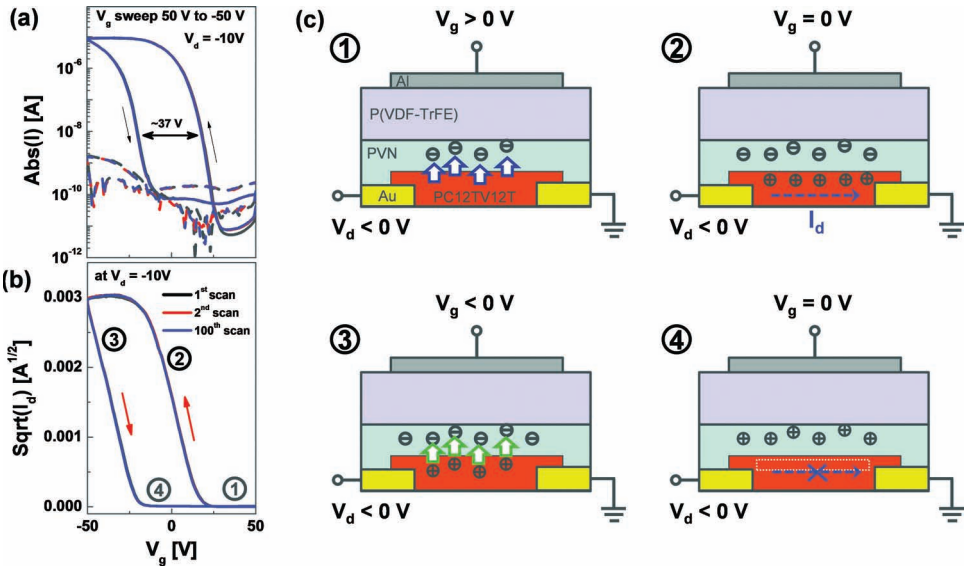

Figure 7. a,b) Reversible bias hysteresis during sequential dual gate voltage sweeps from ±50 V. c) Schematic illustration for the memory operation mechanism at each bias condition indicated in Figure 5b.

PC12TV12T and PVN layers at V_g = 0 V (step-2 in Figure 7c). Stored electrons in the electret layer were completely detrapped by compensation with counter charges (holes), which transferred from the semiconductor to the electret by the application of a reverse-gate bias (step-3 in Figure 7c). Thereafter, the V_{Th} was further shifted in the negative direction beyond the initial value due to re-charging of the excess counter charges (holes) in the PVN layer (step-4 in Figure 7c). It should be noted here that both the transferred electrons and holes were supplied from the PC12TV12T active channel. Debucquoy *et al.* also reported those roles of electrons and holes in the charge trapping of organic transistor memory.[21] The p-channel semiconductor PC12TV12T has weak ambipolar transport characteristics while the majority charge carriers are holes. The electron current in a positive V_g region can obviously be verified in top-gated PC12TV12T OFETs using PS/P(VDF-TrFE) bi-layer dielectrics, as shown in Figure 5b. Although no significant electron current was observed in PVN/P(VDF-TrFE) devices in Figure 5c, it presumably can be assumed that the electrons participated mainly in charge trapping in the PVN electret layer during the programming operation.

Figure 8a,b shows the results of the memory cycling endurance test for the PVN/P(VDF-TrFE) device by sequential application of gate biases of 0 V, 60 V, 0 V, –60 V, and 0 V at V_d = ~20 V, for a series of processes of reading, writing, reading, erasing, and reading, respectively. These results showed reversible and stable memory-cycle behaviour for more than ~10^2 cycles with high I_{on}/I_{off} of ~10^5 at a relatively fast switching time of less than 0.5 s. Note that a relatively high operation voltage can be remarkably decreased by reducing the thickness of the gate dielectrics.[41] The writing voltage was successfully decreased to ~20 V (see Figure 8c) by minimizing the thicknesses of the 1st and 2nd gate dielectric layers [~30 nm thick PVN and ~170 nm thick P(VDF-TrFE) layers] with a range comparable to modern silicon flash memory technology.[42] The thin polymer layers were achieved by careful selection of suitable orthogonal solvents for optimized dielectric film quality. Furthermore, the systematically controllable V_{Th} can be utilized to multi-bit memory cells. By application of suitable gate biases with different ranges, various discrete memory levels can be addressed. As shown in Figure 8d, we obtained two bits per one OFET memory cell by changing the applied gate biases at V_g = 0 V, 12 V, 16 V, and 20 V, for realizing each of the memory states of '00', '01', '10', and '11', respectively. All of these memory states were also quite stable and reversibly changed during the memory cycling endurance tests at V_d = –20 V. The I_{on}/I_{off} between each of the memory levels was more than ~10^1. The multi-bits memory can remarkably increase the memory capacity per unit area, particularly for printed and flexible memory applications frequently requiring relatively large dimensions.

As shown in Figure 8e, the drain current (I_d) was measured at V_d = –20 V and V_g = 0 V after application of different time of gate pulses from 10^{-4} to 5 s under each writing [at V_d = 0, V_g = +20 V] and erasing [at V_d = 0, V_g = –20 V] conditions. The I_d of PC12TV12T OFETs with PVN/P(VDF-TrFE) gradually increased [decreased] from initial off-state [on-state] by increasing the pulse time with proper gate bias of +20 V [–20 V] for programming [erasing] operation, respectively. It is indicated that ±20 V of gate pulses with at least 0.01 s switching time are typically required to fully switch-on or switch-off the memory devices. It should be noted that the switching time is critically depending on the applied gate fields through the gate dielectric layers. Therefore, the switching time can be faster by applying higher gate pulses or by reducing both the electret and blocking gate dielectric thickness. Finally, it is imperative that the retention time be sufficient for long-term stable data storage. Figure 8f shows retention characteristics for both on- and off-current states [Inset: logarithmic time scale plot for estimation of the retention time], where the on- and off-states were measured at V_g = 0 V and V_d = –10 V with a time interval of 60 s after application of V_g = 60 V and –60, respectively, at V_d = 0 V. The initial I_{on}/I_{off} was about 10^5. The stored data (trapped charges in the electret) are stably sustained to the point that the estimated retention time of the PVN/P(VDF-TrFE) memory device was as high as ~10^7 s, which is a relatively long amount of time compared to other types of OFET-based memory devices.[15]

Two major types of flash memory, NAND and NOR, have been considered for a predominant solid-state drive that could be utilized in portable electronic devices, such as MP3 players, mobile phones, and digital cameras.[43] In the circuit configuration of NOR flash, the individual transistor memory cells are connected in parallel, which enables the device to achieve random access and high-speed reading. Therefore, it

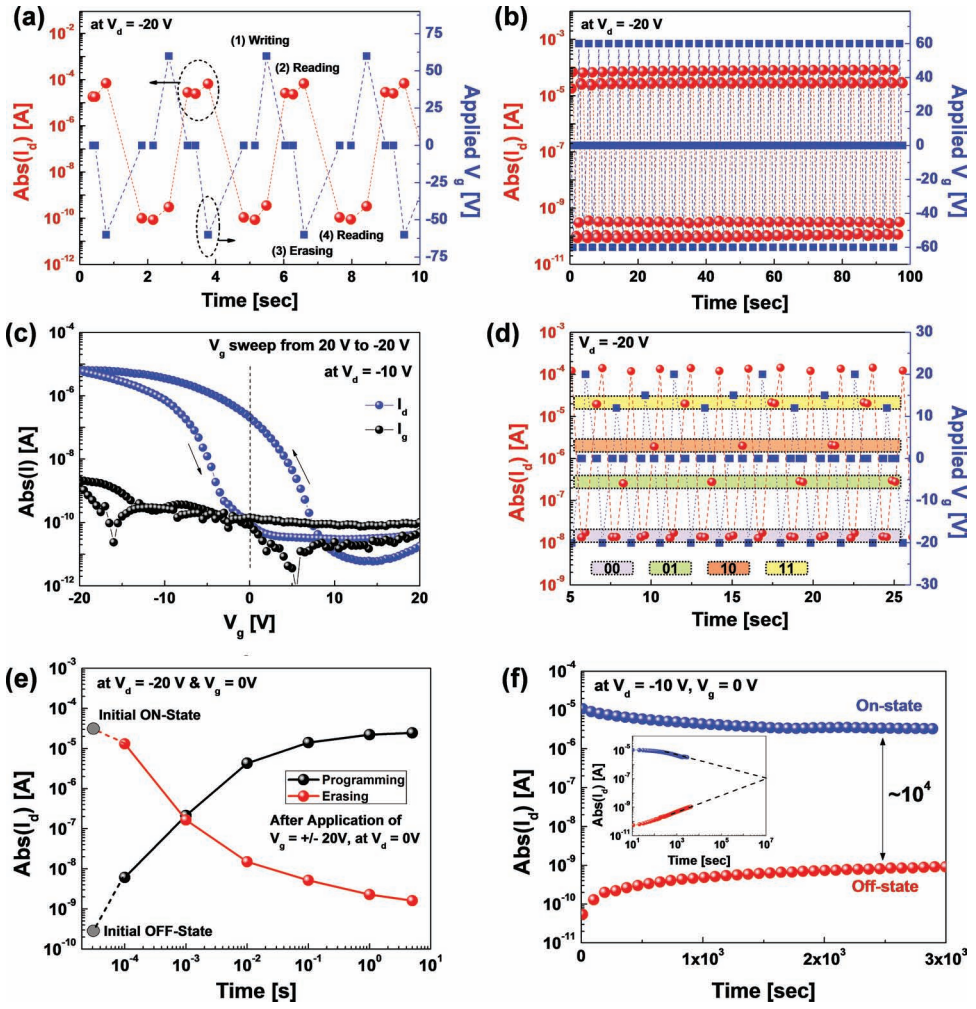

Figure 8. a,b) Memory cycling endurance test: the drain current (I_d) at the on- and off-states were measured at $V_d = -20$ V and $V_g = 0$ V after application of $V_g = 60$ V and $V_g = -60$ V, respectively. c) Low-voltage operating (below 20 V) memory characteristics with thinner gate dielectric layers. d) Multi-level (2 bits/cell) memory characteristics: the I_d at the on- and off-states were measured at $V_d = -20$ V after application of $V_g = 0$, 12, 15, and 20 V for sensing the memory states of "00", "01", "10" and "11", respectively. e) The I_d at the on- and off-states after application of $V_g = 20$ V and $V_g = -20$ V, respectively, for different applied time. f) Retention characteristics of the PVN/P(VDF-TrFE) memory devices (inset: abs(I_d) on a logarithmic time scale).

is suitable for lower-density and read-only memory applications, such as code storage and direct execution in portable electronic devices.[43] In contrast to NOR type, NAND flash memory was developed as an alternative optimized for high-density data storage media, in which random access capability is given up in a trade-off to achieve a smaller cell size.[43] This is usually achieved by creating an array of eight or sixteen transistor memories connected in a series where each array has one end directly grounded and the other end connected directly to a bit line.[43] NAND flash is believed to be a more appropriate architecture for printed organic memory devices than the NOR type since NAND flash has a simpler architecture with fewer ground wires and bit lines.[19] This provides greater storage capacity per unit area as printed-features using conventional graphic art printing processes show are typically large-scale and their minimum line width and pitch are more than a few tens μm.[42] Moreover, greater fault tolerance and moderate switching speeds required in NAND flash are considered to be suitable for printed organic transistor-type memory, which typically shows lower charge carrier mobility and less manufacturing yield than silicon-based semiconductor memory. Therefore, the printed organic NAND flash memory is believed to be the best candidate for use in flexible electronic products when its memory performance fulfils the required specifications.

NAND flash memory consists of independent blocks, which are considered to be the smallest erasable units and pages that are the smallest programmable units. As represented in Figure 11a, the basic block architecture consists of many pages and bits, a bit array has normal transistors for bit-line or ground selection and many memory cells (typically floating-gate transistor memories). In the present study of top-gated OFETs with bi-layer gate dielectrics, a suitable selection of the 1st gate dielectrics could change the OFET device operation modes either to normal transistor (using PS) or to non-volatile memory (using PVN), respectively. The fabrication

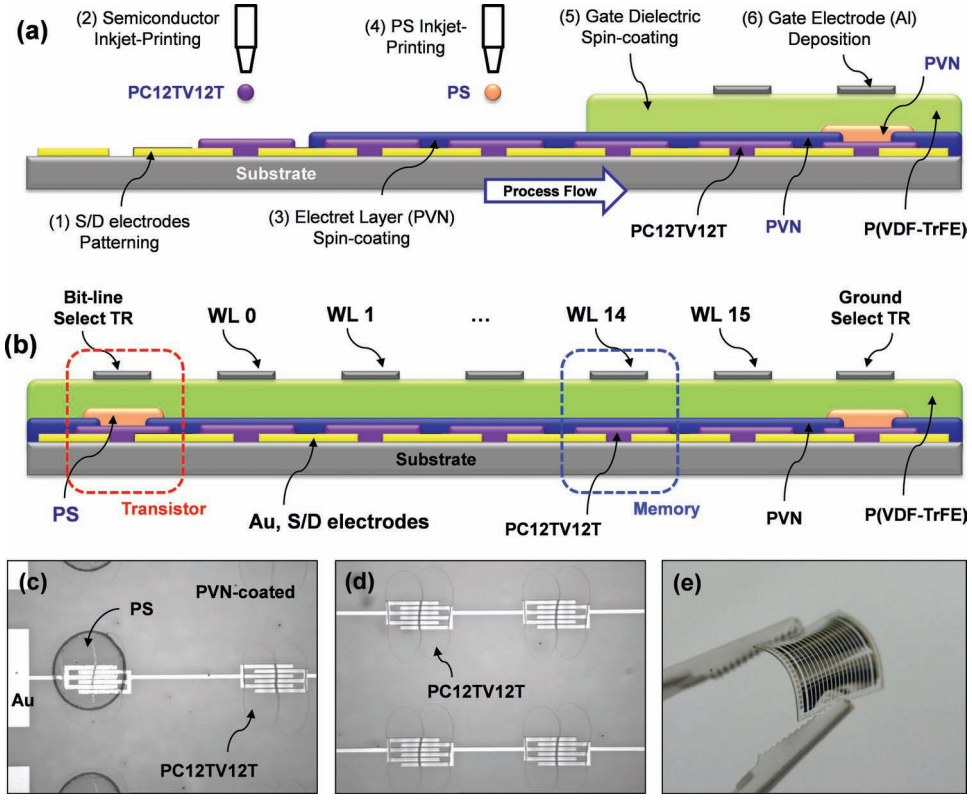

Figure 9. Facile strategy for development of flexible printed organic NAND flash memory. a) Schematic diagram of fabrication process flow and b) schematic illustration of a cross-sectional view of the 256-bit NAND-type organic flash memory. CCD camera images: c) of PS inkjet-printed onto PVN and PC12TV12T layers and d) inkjet-printed PC12TV12T active feature and spin-coated PVN layer above the PC12TV12T. e) Digital camera image of the fabricated flexible printed organic flash memory on a PEN substrate.

process flow is schematically represented in **Figure 9**a, and Figure 9b shows the cross-sectional schematic configuration of flexible printed organic NAND flash where the PVN was spin-coated above the inkjet-printed PC12TV12T polymer semiconductor, and the PS ink (~5 mg/ml in n-butylacetate, nBA) was inkjet-patterned onto the PVN-coated transistor regions. As shown in Figure 9c, PS was inkjet-printed onto the PVN and PC12TV12T layers, where the PVN was partially removed and PS was upper-deposited mainly on PC12TV12T, since the nBA solvent in the printed PS droplet marginally dissolved the PVN layer. Therefore, the PS/P(VDF-TrFE) OFET devices carried out normal transistor operation as bit-line or ground-select transistors, while the PVN/P(VDF-TrFE) OFET devices functioned as floating-gate-like memory cells under the same bias conditions.

As shown in **Figure 10**b,c, the PS/P(VDF-TrFE) and PVN/P(VDF-TrFE) devices, respectively, exhibited completely different bias hysteresis behaviours under the same V_g sweep conditions (forward and reverse gate bias scans between 30 V and −30 V at V_d = −20 V). Only the PVN/P(VDF-TrFE) device had a significant MW of ~20 V with a high I_{on}/I_{off} of ~10^5, while the PS/P(VDF-TrFE) devices had no significant opened MW. Moreover, the inkjet-printed organic NAND flash memory using top-gated OFETs and electret were demonstrated on a plastic substrate, polyethylene naphthalate (PEN, DuPont Tenjin Films), as shown in Figure 9e. For a flexible memory application on a plastic substrate, the PC12TV12T semiconductor was thermal annealed at a moderate temperature of ~120 °C, for which the μ_{FET} was degraded to ~0.02 cm^2/Vs than that of annealed device at 200 °C, but the other memory characteristics such as MW and I_{on}/I_{off} were not significantly affected.

Reproducible programming, erasing, and reading characteristics of the flexible printed NAND flash memory array are verified by electrical simulations. All circuit simulations were performed with H-Spice circuit simulator and the circuit model parameters, which based on measured n-type transistor (see Figure 10a, P(NDI2OD-T2) OFET with PS/P(VDF-TrFE)), p-type transistor (see Figure 10b, PC12TV12T OFET with PS/P(VDF-TrFE)), and non-volatile memory (see Figure 10c, PC12TV12T OFET with PVN/P(VDF-TrFE)) characteristics. In order to simulate a flexible printed organic NAND flash memory circuit, the current-voltage characteristics of these devices are modeled, as shown in Figure 10d–f. The gate capacitors of 5.14pF are included in the circuit models for the accurate transient simulation. **Figure 11** shows the circuit schematic of the 256 bit flexible printed organic NAND Flash memory. 16 non-volatile memory cells are connected to 16 word lines (WL0–WL15). The NAND flash memory cell block is enabled by two p-type transistors connected to bit line (BL) select signal and ground (GND) select signal, respectively. The decoder and word line driver circuits

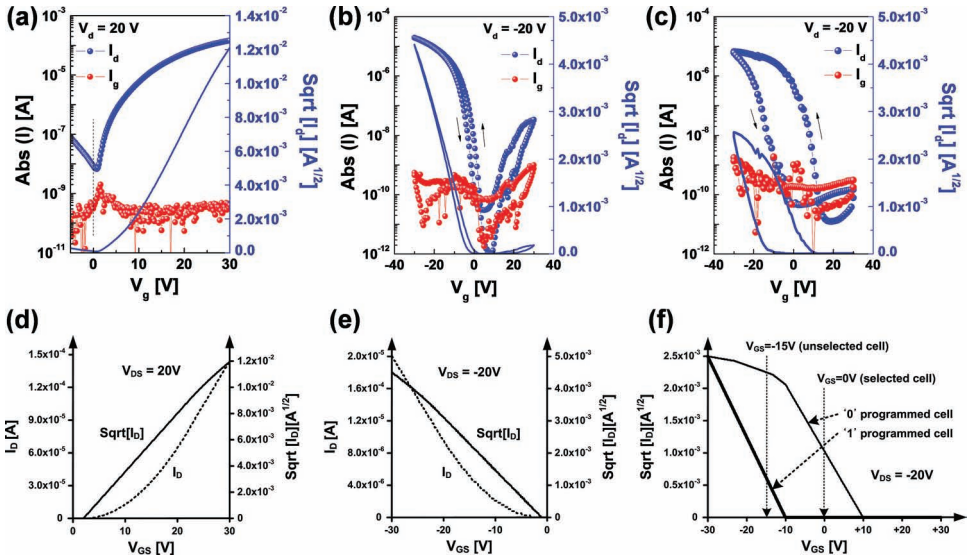

Figure 10. Representative measured transistor data: a) normal n-type transistor [P(NDI2OD-T2) OFET with PS/P(VDF-TrFE)], b) normal p-type transistor [PC12TV12T OFET with PS/P(VDF-TrFE)], and c) non-volatile memory [PC12TV12T OFET with PVN/P(VDF-TrFE)] characteristics. Simulated transistor characteristics of the circuit models of flexible printed organic devices: d) n-type transistor, e) p-type transistor, and c) non-volatile memory.

make the word line signals and control signals from −40 V to +40 V. The signal voltages according to the operation modes (erase, write, and read) are summarized in **Table 2**.

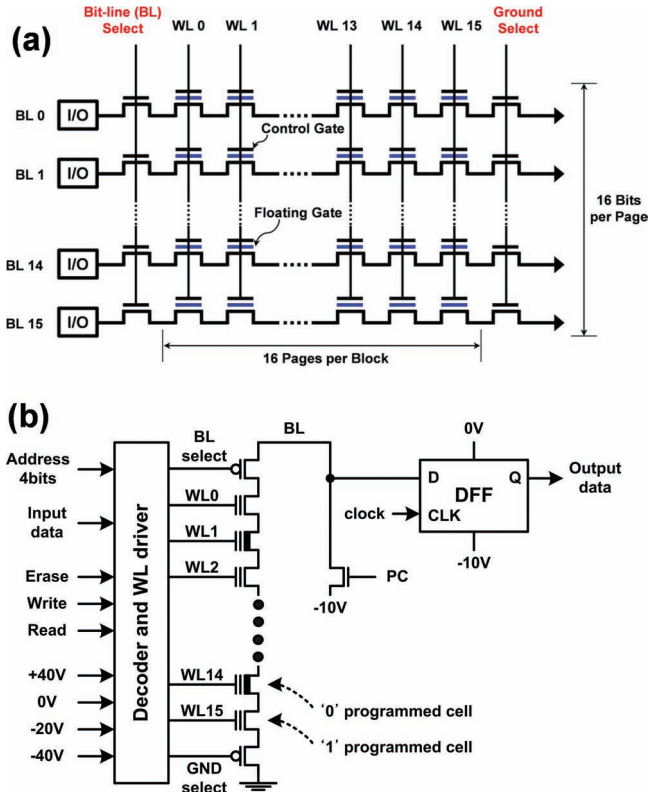

Figure 11. a) 256 Bit (16 × 16 array) NAND flash memory circuit diagram and b) circuit schematic for measuring electric data of a flexible printed organic NAND Flash memory.

Figure 12 shows the simulated waveforms of the flexible printed organic NAND Flash memory. At erase mode, all cells are programmed to '0' by applying −40 V to their WLs during 0.5 s, as shown in Figure 12a. And then, at write mode, 16 memory cells are sequentially programmed according to the input data. If the input data is '1', the selected memory cell is programmed to '1' by applying +40 V to its WL during 0.5 s. If the input data is '0', the WL voltage of the selected cell is 0 V and the selected cell data remains at '0'. The read operation is much faster than the erase and write operations. The read access time is 40 ms, as shown in Figure 12b. During the read mode, 16 memory cell data are sequentially accessed. The selected word line is 0 V and the other word lines are all −15 V. As shown in Figure 10f, the V_g of the selected memory cell is 0 V and the selected memory cell turns on or off according to the stored data. The V_g of all unselected memory cells are −15 V and the memory cells turn on independent of their stored data. Therefore, if the selected memory cell stores '0', the NAND memory cell block composed of 16 memory cells and two p-type transistors is connected to ground. If not, the block is disconnected from ground. To read the data in selected memory cell, the BL is pre-charged to −10 V by the pre-charge (PC) signal during 4 ms. And then, if the data stored in the selected cell is '0', the bit line is charged to 0 V, because the NAND memory cell block is connected to ground. But, if not, the bit line remains at −10 V, because the NAND memory cell block is disconnected from ground. The data in the BL is latched by the data flip-flop (DFF) to make the output data. The logic circuits use 0V and -10V for logical '1' and '0', respectively. From these circuit simulations, the monolithically printed normal OFETs [PS/P(VDF-TrFE) devices] and floating-gate-like electret memory cells [PVN/P(VDF-TrFE) devices] reveal to be a promising strategy for development of flexible printed organic NAND flash memory.

Table 2. The signal voltages for simulation of the flexible printed organic NAND Flash memory.

Operation mode			Erase	Write	Read
Nonvolatile Memory	Selected cell	Gate (WL)	–40 V ('0' program)	+40 V ('1' program)	0 V (No program)
		On/off state	On	Off	On @ '0' cell Off @ '1' cell
	Unselected cell	Gate (WL)	N/A (All cells are selected)	–15 V (No program)	–15 V (No program)
		On/off state		On @ all cells	On @ all cells
BL select (PMOS)		Gate	0 V (Off)	0 V (Off)	–20 V (On) 0V (Off)
GND select (PMOS)		Gate	–20 V (On)	–20 V (On)	–20 V (On)
Pre-charge (NMOS)		Gate (PC)	0 V (On)	0 V (On)	0 V (On) –10 V (Off)

3. Conclusions

In conclusion, we have outlined a facile strategy for the development of monolithically printed and flexible organic NAND flash memory by using electrets in top-gated OFETs. The PC12TV12T OFETs devices with PVN/P(VDF-TrFE) bi-layered top-gate dielectrics showed excellent non-volatile memory characteristics: a large MW of more than 90 V, a high I_{on}/I_{off} of ~10^5, a stable and reversible memory cycling endurance of more than 10^2 cycles, a relatively low operation voltage of less than 20 V, a relatively short switching time of less than 0.01 s, a long retention time of ~10^7 s, and multi-level (2 bits per one cell) memory capability. The superior memory characteristics originated mainly from reversible charge trapping and detrapping in the PVN electret layer efficiently in low-k/high-k bi-layered dielectric layers. In contrast, The PS/P(VDF-TrFE) devices showed negligible MW under low-bias conditions and a narrow MW of ~34 V even at a high applied gate bias of more than ±90 V. After suitable selection of the electret layer materials (PVN or PS), a monolithically printed and flexible organic NAND flash memory array can be produced for selected operation as normal transistor (using PS) or memory cells (using PVN). We strongly believe that commercialized printed flash memory can begin in the near future using OFETs with polymer electrets.

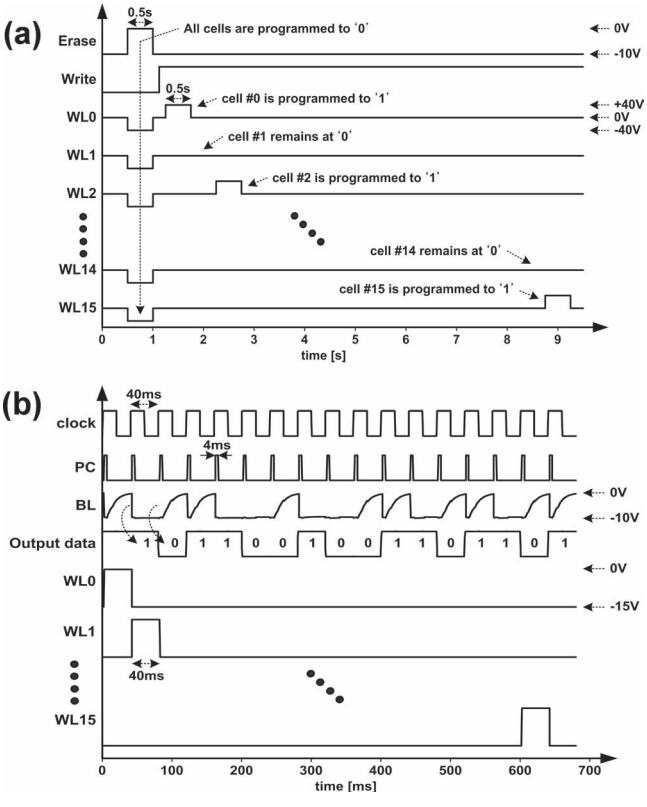

Figure 12. Simulated waveforms of a flexible printed organic NAND Flash memory: a) erase and write mode and b) read mode.

4. Experimental Section

Device Fabrication: The Au/Ni (15 nm/3 nm thick) patterns used for the S/D electrodes were fabricated using a conventional photolithography procedure on Corning Eagle 2000 glass and PEN (Tenjin DuPont Films) plastic substrates. The substrates were cleaned with deionized water, acetone, and 2-propanol in an ultrasonic bath for 10 min each. PC12TV12T was synthesized in our laboratory,[24] and dissolved in anhydrous p-xylene to obtain ~3 mg/ml of solution. The solution was then filtered via a 0.2 μm polytetrafluoroethylene (PTFE) syringe filter before use. The semiconductor solution was inkjet-printed onto Au/Ni patterned substrates in air while maintaining the substrates at room temperature using a custom-built research inkjet printer (UJ200MF, Unijet, Korea). A piezoelectric-type drop-on-demand dispensing head (Microfab Tech.) with a 50 μm orifice diameter was used at an operating frequency of 1 KHz. The semiconductor film was thermally annealed at 200 °C (at 120 °C for PEN substrate) for 30 min in a N_2-purged glove box. PS and PVN were purchased from Aldrich and used without further purification, and dissolved in 2-butanone or nBA for proper usage (5–10 mg/ml concentration). Random copolymer P(VDF-TrFE) (70:30 mol%) was purchased from Solvay Chemicals and dissolved in acetonitrile to obtain a 30–50 mg/ml concentration solution. The PS and PVN were spin-coated at 5000 rpm onto PC12TV12T inkjet-patterned substrates, and slightly baked at 80 °C for 10 min in N_2 glove box. The P(VDF-TrFE) was spin-coated at 2000 rpm onto PS or PVN-coated samples with subsequent thermal annealing at 80 °C for 30 min in N_2 glove box. The transistors were completely fabricated by depositing the aluminium (Al) top-gate electrodes (~35 nm) via thermal evaporation using a metal shadow mask.

Characterization: The current-voltage characteristics of the OFETs and memory devices were measured using a Keithley 4200-SCS in a

N_2-purged glove box. The gate dielectric capacitance and dielectric constants were measured using a Keithley 4200 at 100 KHz. The surface profile was measured using a surface profiler (Ambios, XP-1) after scratching the 1st and 2nd layers after coating onto the substrate. The surface morphology of the films was investigated via tapping-mode AFM (Nanoscope III, Veeco Instruments, Inc.) at the Korea Basic Science Institute (KBSI). All circuit simulations were performed with H-Spice circuit simulator and the circuit model parameters, which based on measured transistors and memory characteristics.

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